Applicant : Muraleedhara Navada et al. Attorney's Docket No.:10559-906001

Serial No.: 10/750,554

Filed : December 31, 2003

Page 2 of 6

Amendments to the Specification:

Please replace the paragraph beginning at page 1, line 21, with the following amended paragraph:

 $\overline{\text{FIG. 3 is}}$ $\overline{\text{FIGS. 3A}}$ and $\overline{\text{3B}}$ are a block diagram depicting a stack of routers.

Please replace the paragraph beginning at page 10, line 22, with the following amended paragraph:

Referring to FIG. 3 FIGS. 3A and 3B, each of the routers 28-34 in the stack respectively includes six ports (e.g., ports 1-6) that allow bi-directional packet transferring among the routers. For example, port 3 in router 28 connects to port 1 in router 30 for transferring packets. Similarly, port 6 in router 30 connects to port 4 in router 32 for transferring packets in either direction. Also, port 2 in router 30 connects to port 5 in router 34. Since exception packets from each of the routers 28-32 are sent to router 34 for delivery to exception handler 36, three ports (e.g., ports 1, 2, and 3) in router 34 connect to three ports (e.g., ports 1, 2, and 3) in the exception handler. By connecting router 34 and exception handler 36 with multiple transmission lines, the appropriate bandwidth is

Applicant : 'Muraleedhara Navada et al. Attorney's Docket No.:10559-906001

Serial No.: 10/750,554

Filed : December 31, 2003

Page 3 of 6

provided to handle the combined exception packet traffic from each router.

Please replace the paragraph beginning at page 13, line 23, with the following amended paragraph:

After packet 2 is received by router 28, the router determines that packet 2 is associated with an exception and needs to be sent to exception handler 36. To direct packet 2 through the stack to exception handler 36, router 28 produces exception packet 2 that is labeled "E 2" in FIG. 3A. Router 28 also inserts a device vector 78 in exception packet 2 that identifies router 34 as the destination of the packet by storing a logic "1" in the respective device vector bit 80 assigned to router 34. Also, to identify exception_packet_2 as an exception packet, a logic "1" is stored in exception flag 82 included in the packet header. Once device vector 78 and exception flag 82 are inserted into exception packet 2, the packet is sent out port 3 of router 28 to router 30. By examining the inserted device vector, router 30 determines that exception packet 2 is intended for router 34 and sends the packet through port 2 to port 5 in router 34. Router 34 determines which of the three ports (e.g., port 1, 2, or 3) to use to send exception_packet_2 to exception handler 36.

Applicant : Muraleedhara Navada et al. Attorney's Docket No.:10559-906001

Serial No.: 10/750,554

Filed : December 31, 2003

Page 4 of 6

Please replace the paragraph beginning at page 14, line 17, with the following amended paragraph:

Similar to packet 2, router 32 determines that received packet 3 is associated with an exception and produces an exception packet 3, labeled in FIG. 3 FIG. 3B as "E 3", which needs to be sent to exception handler 36 for processing. direct exception packet 3 through the stack and to exception handler 36, router 32 inserts a device vector 84 in exception packet 3 that stores a logic "1" in bit 86, which is assigned to identify router 34. Also, to identify exception_packet_3 as an exception packet, a logic "1" is stored in an exception flag 88 that is inserted in exception packet 3. Once device vector 84 and the exception flag 88 are stored in exception packet_3, the packet is sent through port 4 of router 32 to router 30. After receiving exception packet 3, router 30 determines from device vector 84 that the packet is destined for router 34 and sends it through port 2 to router 34. After receiving exception packet 3, router 34 determines which one of its ports 1, 2, or 3 to send the packet for processing by an exception processor 90, for example an Intel® IXP 2800 Network Processor, which is included in exception handler 36. Also, the

Applicant : Muraleedhara Navada et al. Attorney's Docket No.:10559-906001

Serial No.: 10/750,554

Filed : December 31, 2003

Page 5 of 6

exception handler 36 typically includes a memory 92 that stores packets prior to their processing by exception processor 90.

Please replace the paragraph beginning at page 22, line 16, with the following amended paragraph:

To direct exception packets to exception handler 36, the device vector inserted in the exception packet is accessed by the packet forwarder executed in the recipient router to determine which bits are set to logic "1" and uses the locally stored exception routing table stack to determine which stack device (e.g., router 34) is dedicated to sending exception Then, the locally stored packets to exception handler 36. stack device table is accessed to determine the particular port or ports to send the packet or copies of the packet. For example, when exception packet 2 (shown in FIG. 3 FIG. 3A and labeled "E 2") is received by router 30, the exception packet manager executed in router 30 accesses the exception routing table 120 and determines that exception packet 2 is to be sent to router 34 for delivering to exception handler 36. The packet forwarder executed on router 30 determines from stack device table 112 that the exception packet 2 is to be sent over port 2 for routing to router 34.